Clock Jitter Effect for Testing Data Converters

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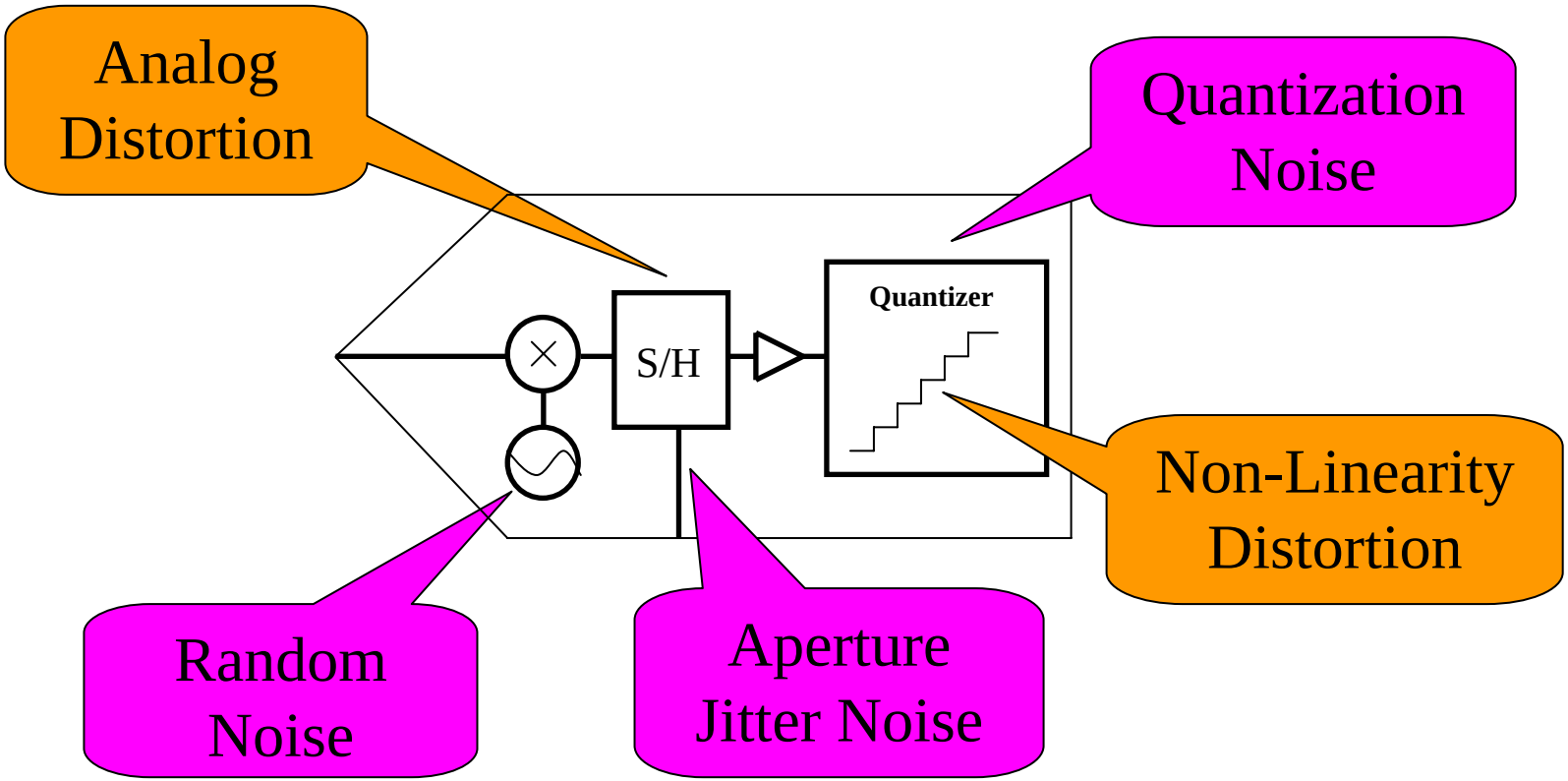
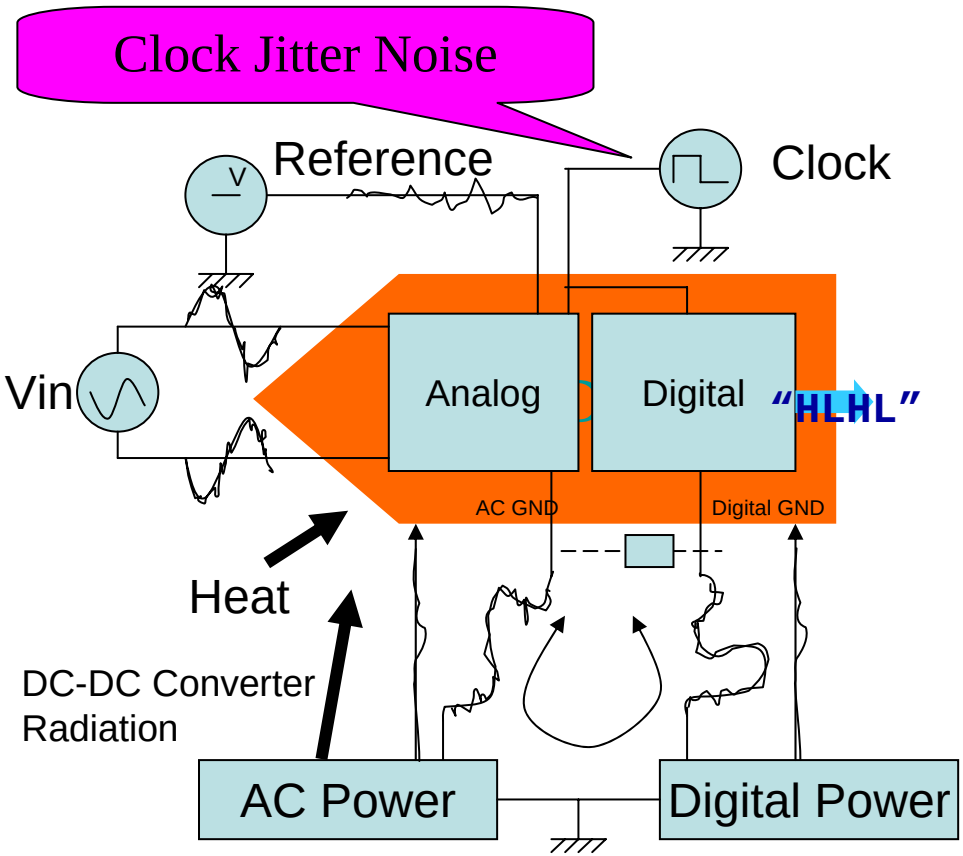
- Calculation of SNR with Clock Jitter
  - Minimum Clock Jitter for Testing N bit Data Converter
  - Table for Clock jitter, input signal and ENOB
- Simulation of Clock Jitter Effect using 14 Bit DAC and Input Signal Model.
- Real SNR Testing for 14 Bit DAC by Adding Clock Jitter

Model & Parameters to Data Converter Measure

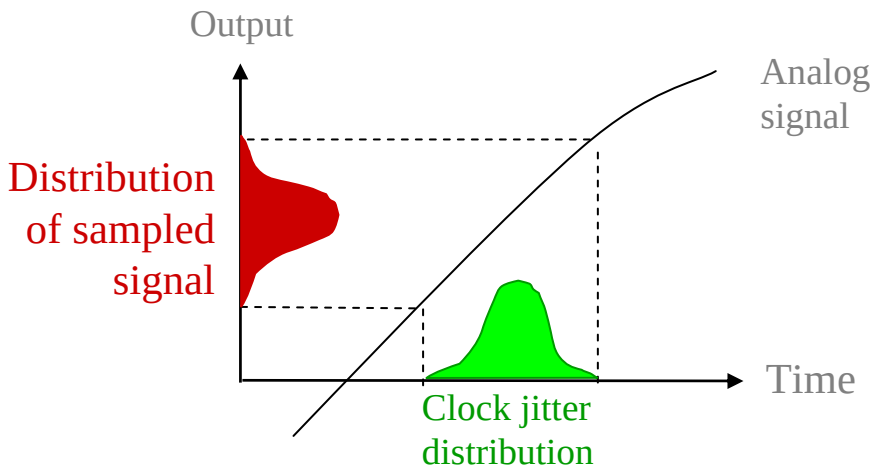


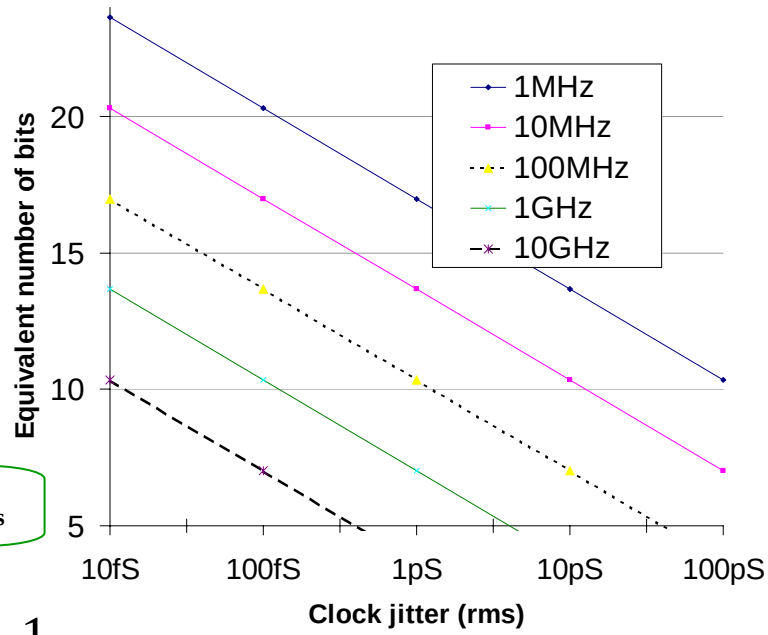
Sources of Noise for Testing Data Converter

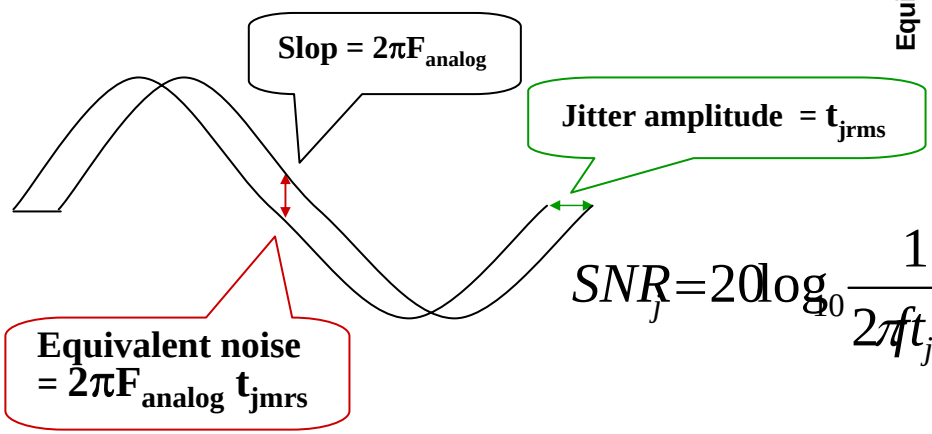


- Non-linearity of Data Converter
- Reference Pin Noise
- Input Signal Jitter, Distortion and Noise
- Clock Jitter
- Data Jitter
- Data Signal Power Feedback
- Clock Signal Power Feedback
- Power and Ground Noise
- Separated Ground Plane Loop Noise Pick-up
- AC Power 60Hz/50Hz Noise
- DC-DC Converter Switching Noise
- Thermal Noise

Jitter Effect in Time Domain







$$SNR_j = 20\log_{10}\frac{1}{2\pi f t_{jrms}}$$

SNR of Data Converter with Clock Jitter Component

$$SNR = 10 \log \left[(2*PI*Fi*Tj)^2 + (10^{SNR_{ideal}/20})^2 \right]$$

$SNR_{ideal} = -(6.02 * N + 1.76)$ dB

N : Data Converter Bit size

Fi : Conversion Frequency

Tj : RMS Jitter of Conversion Clock

Minimum Clock Jitter for Testing N-bit Data Converter

$$Tj = 10^{SNR\ ideal/20} / (2*PI*Fi)$$

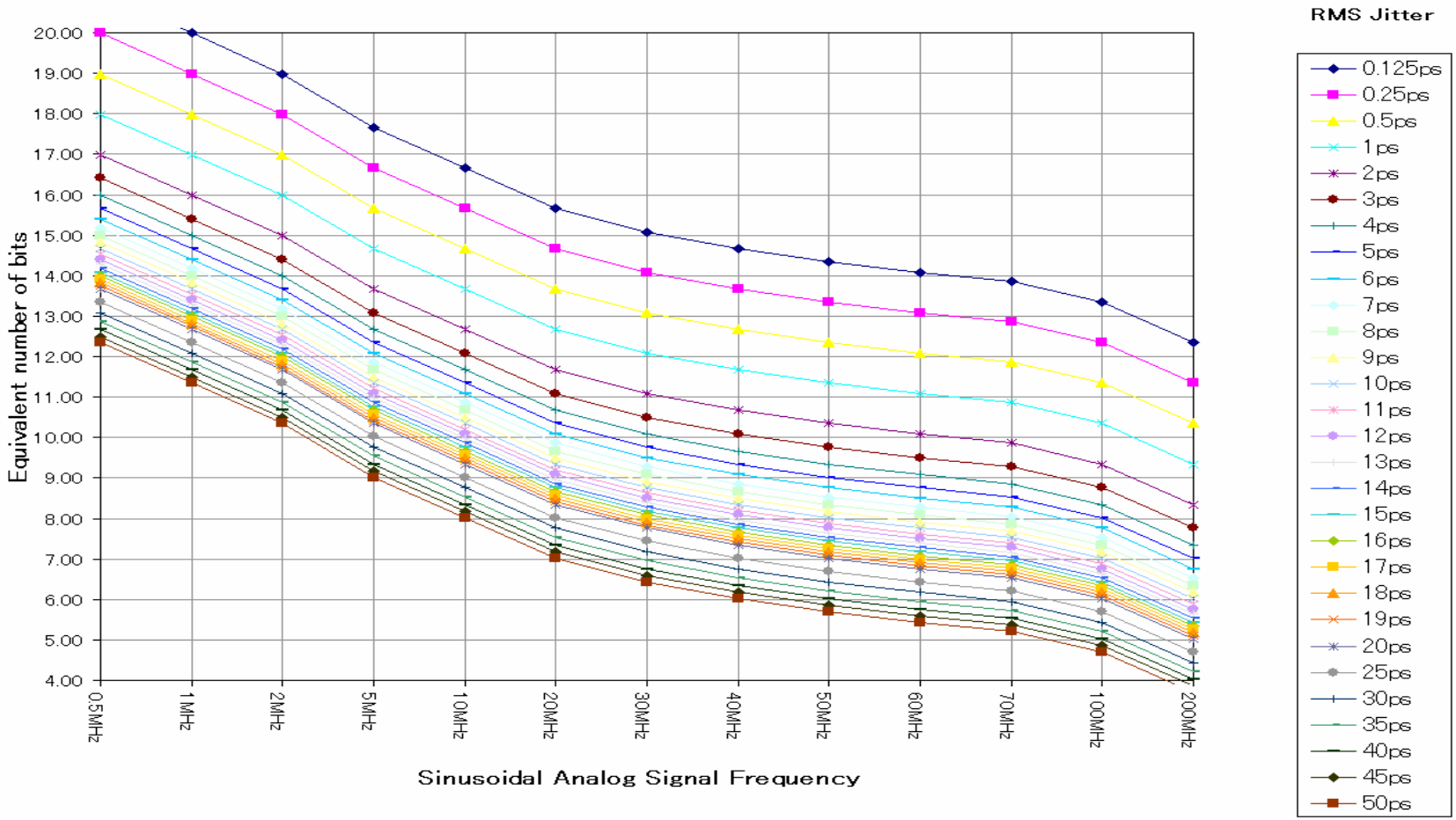
SNR ideal = -(6.02 * N + 1.76) dB

N : Data Converter Bit size

Fi : Conversion Frequency

Tj : RMS Jitter of Conversion Clock

Theoretical Jitter to ENOB Table

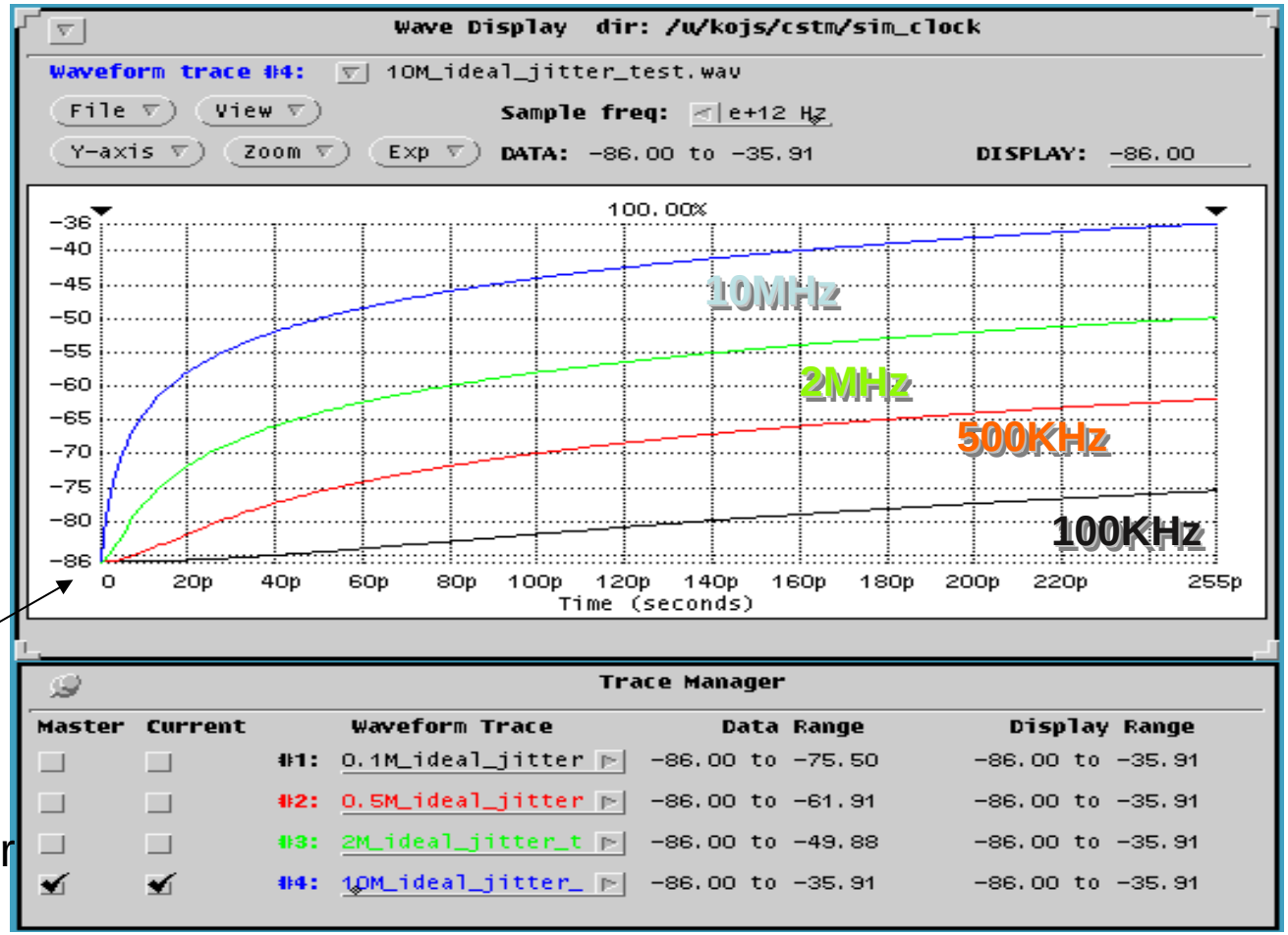


SNR of 14 bit Data Converter

- SNR of Ideal 14 bit data converter is 86.04 dB
- Sweep Random Clock Jitter Tj from 0 to 255ps by 1.0ps step
- Calculate SNR for 100KHz, 500KHz, 2 MHz and 10MHz Signal

$$SNR = 10 \log \left[(2*PI*Fi*Tj)^2 + (10^{SNR_{ideal}/20})^2 \right]$$

SNR Calculation Data by Clock Jitter



14 bit
SNR 86.04dB
with 0 Clock jitter

Simulation Model of the Jitter Effect

- Create Ideal N-bit Sine Wave Signal Function
- Add RMS Jitter Noise Tj to Sampling Clock Fs

$$F(t) = \sin [2*PI*Fi*(t+Tj)/Fs]$$

- Calculate SNR for Fi 2Mhz Signal for 0-100psrms Clock Jitter

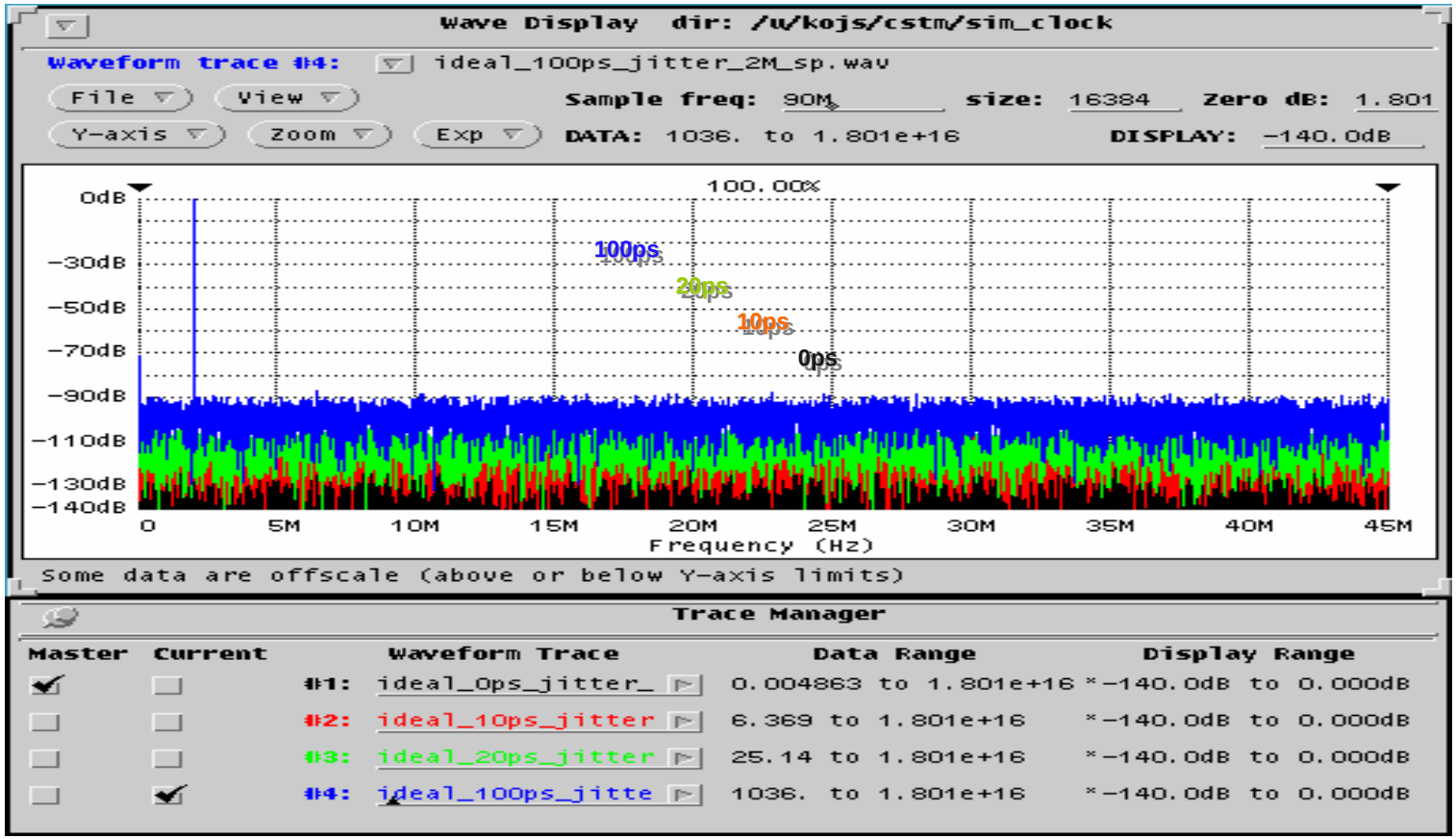
Simulation Result

Text Editor V3.5.1 - jitter_ideal_2M_SNR.txt, dir; /u/kojs/cstm/sim_clock

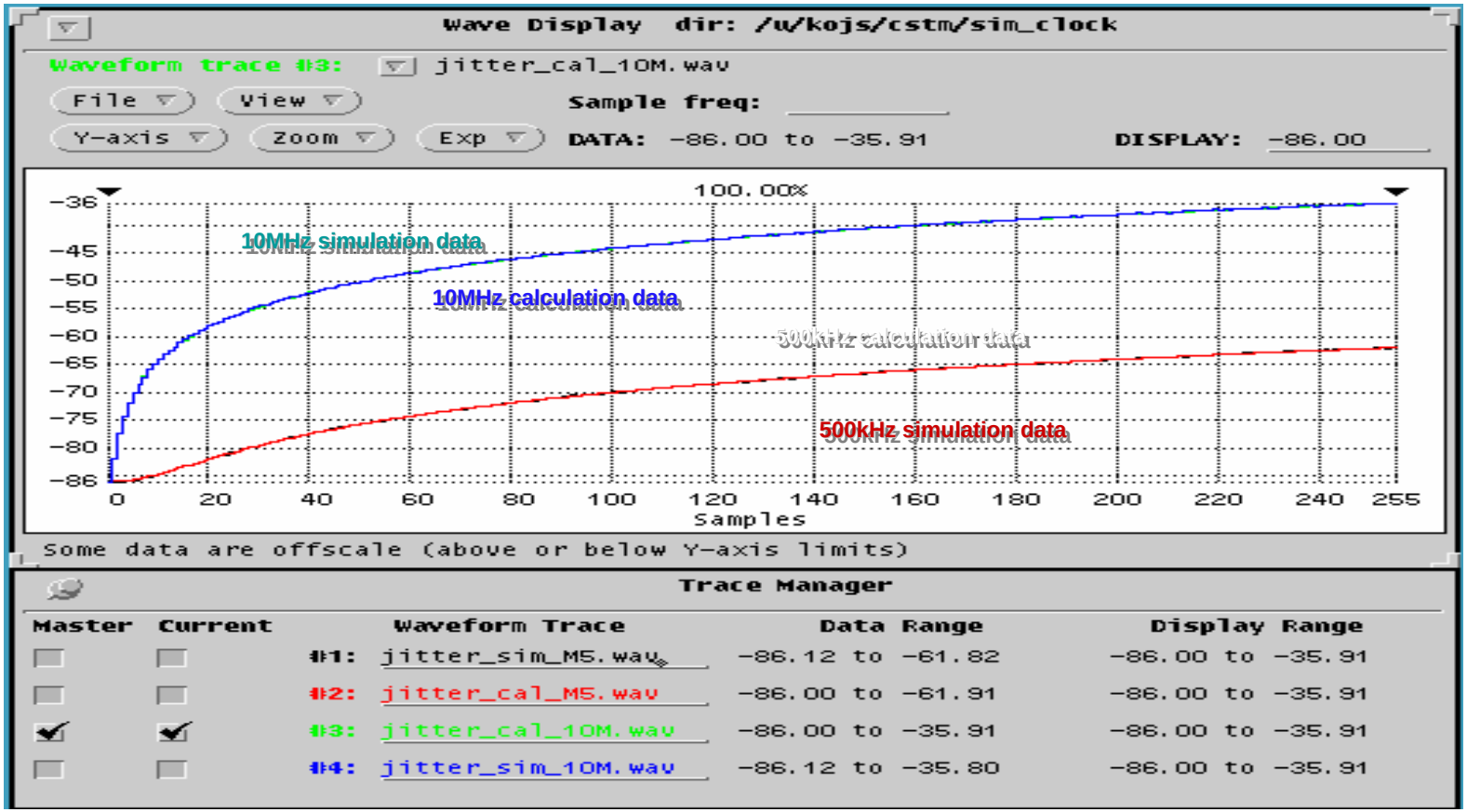
File View Edit Find

```
Seg_size      DIBSRC_Freq          DIBSRC_Clock         Clock_Jitter
N = 16384     Fi = 2.005005 MHz    Fs = 90.00000 MHz    Tj =  0.00 psrms
-------------------------------------------------------------------------------
SNR  =  86.119 dB     ENOB   = 14.013 bits
SFDR = 110.767 dB     F_Spur = 21066.284 kHz
H_2nd=-156.535 dBc    H_3rd  =-118.448 dBc            THD = -117.144 dB

Seg_size      DIBSRC_Freq          DIBSRC_Clock         Clock_Jitter
N = 16384     Fi = 2.005005 MHz    Fs = 90.00000 MHz    Tj = 10.00 psrms
-------------------------------------------------------------------------------
SNR  =  77.320 dB     ENOB   = 12.551 bits
SFDR = 106.912 dB     F_Spur = 41605.225 kHz
H_2nd=-113.155 dBc    H_3rd  =-119.335 dBc            THD = -108.463 dB

Seg_size      DIBSRC_Freq          DIBSRC_Clock         Clock_Jitter
N = 16384     Fi = 2.005005 MHz    Fs = 90.00000 MHz    Tj = 20.00 psrms
-------------------------------------------------------------------------------
SNR  =  71.760 dB     ENOB   = 11.628 bits
SFDR = 101.163 dB     F_Spur = 1878.662 kHz
H_2nd=-114.088 dBc    H_3rd  =-112.261 dBc            THD = -103.477 dB

Seg_size      DIBSRC_Freq          DIBSRC_Clock         Clock_Jitter
N = 16384     Fi = 2.005005 MHz    Fs = 90.00000 MHz    Tj = 100.00 psrms
-------------------------------------------------------------------------------
SNR  = 57.931 dB      ENOB   = 9.331 bits
SFDR = 87.073 dB      F_Spur = 6427.002 kHz
H_2nd=-90.397 dBc     H_3rd  =-93.729 dBc             THD = -86.995 dB
```

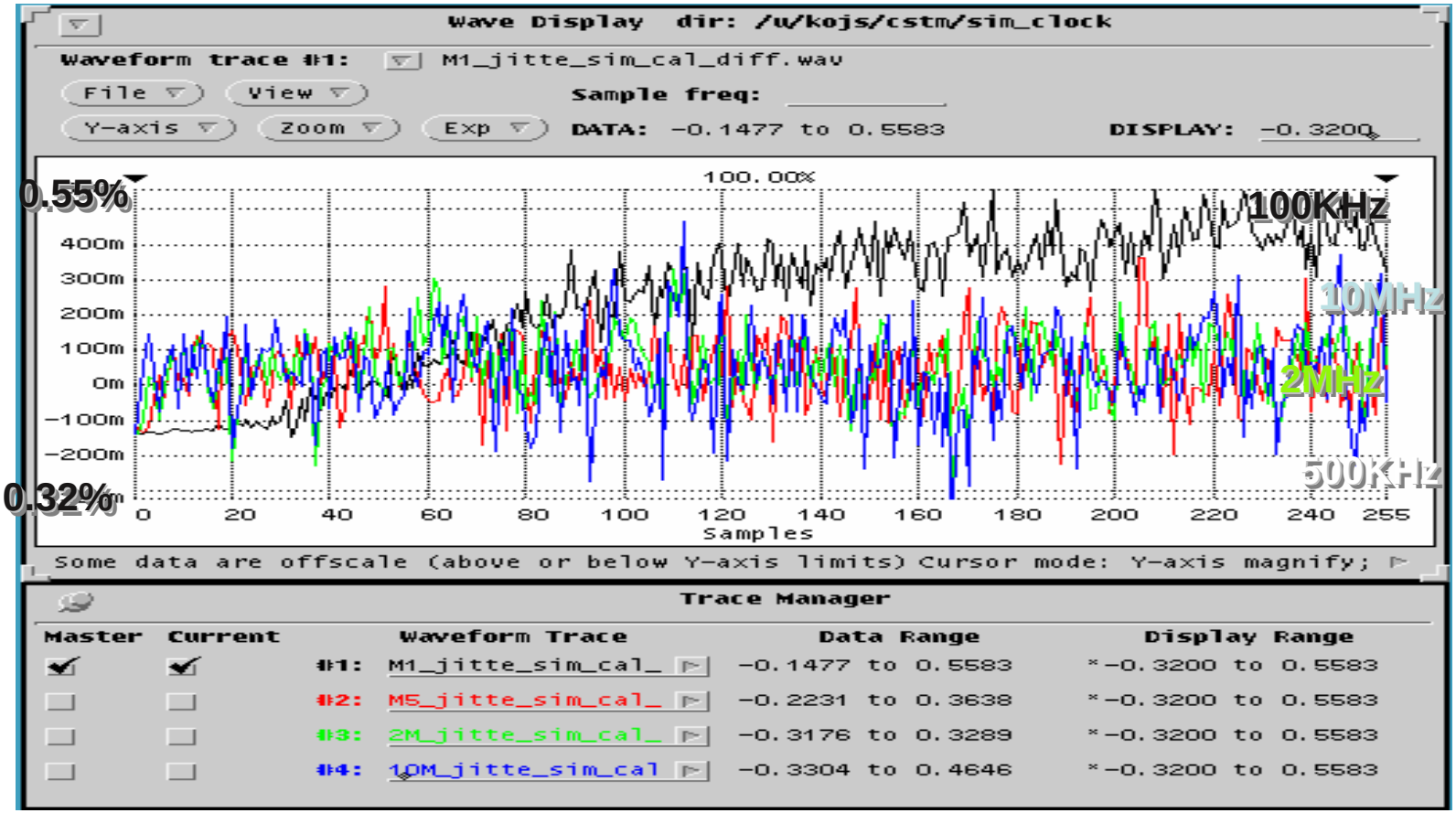
Power Spectrum View of the 14-bit Converter Simulation Model



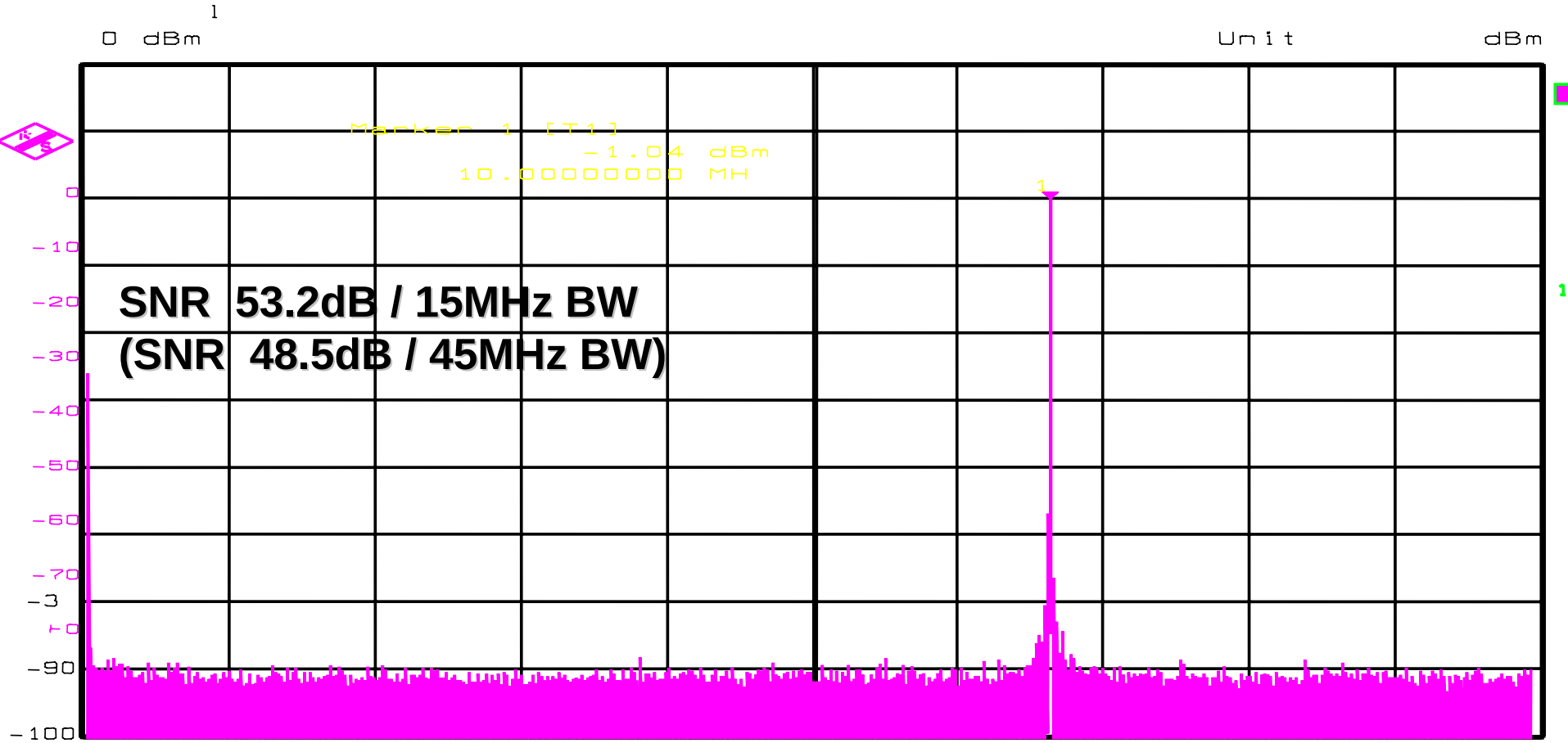
SNR Data Overlap of the Calculation and Simulation data



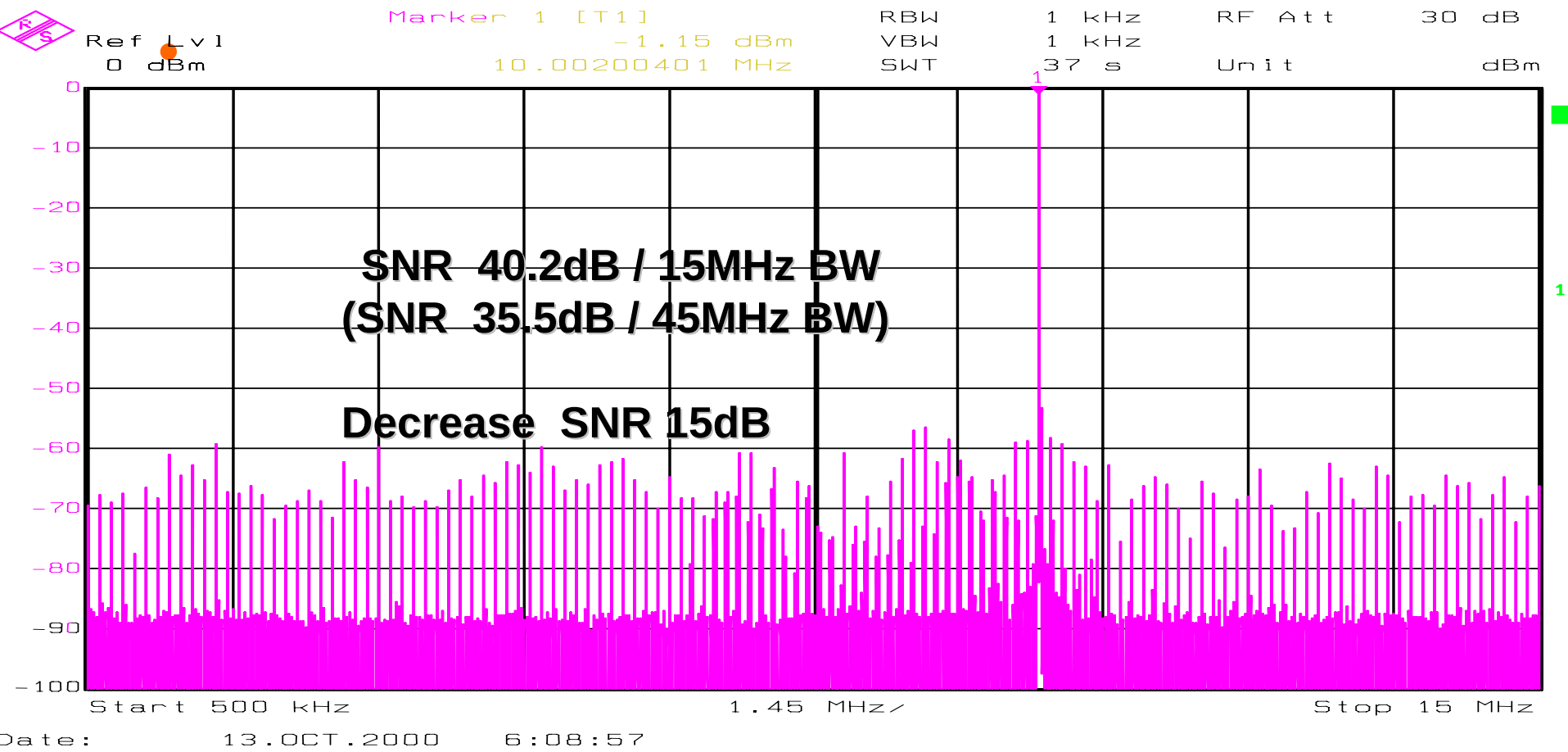
SNR Data Difference Between The Calculation and Simulation Data



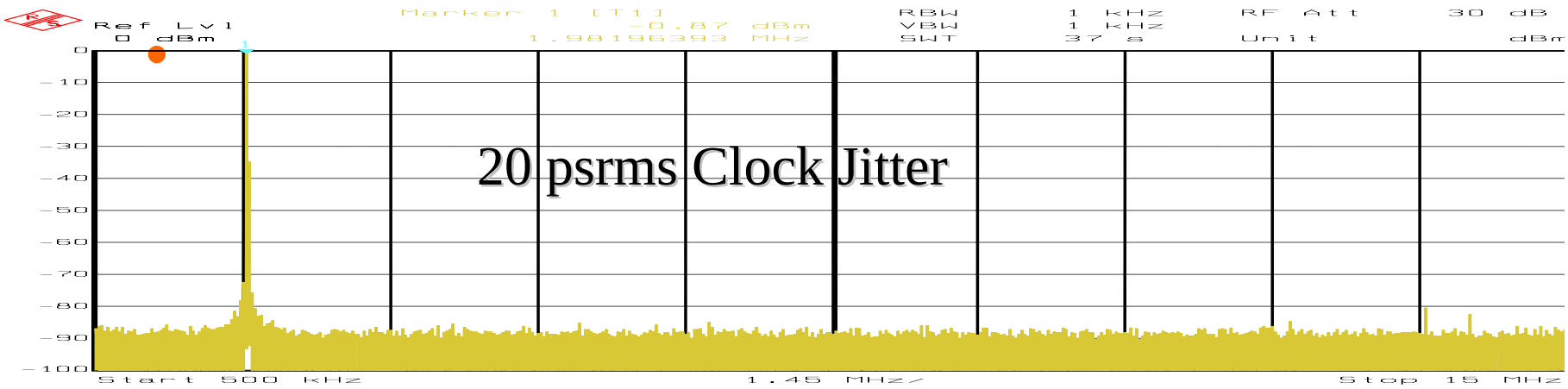
Fi 10Mhz , Clock Jitter 20psrms
Power Spectrum of 14 bit ADC



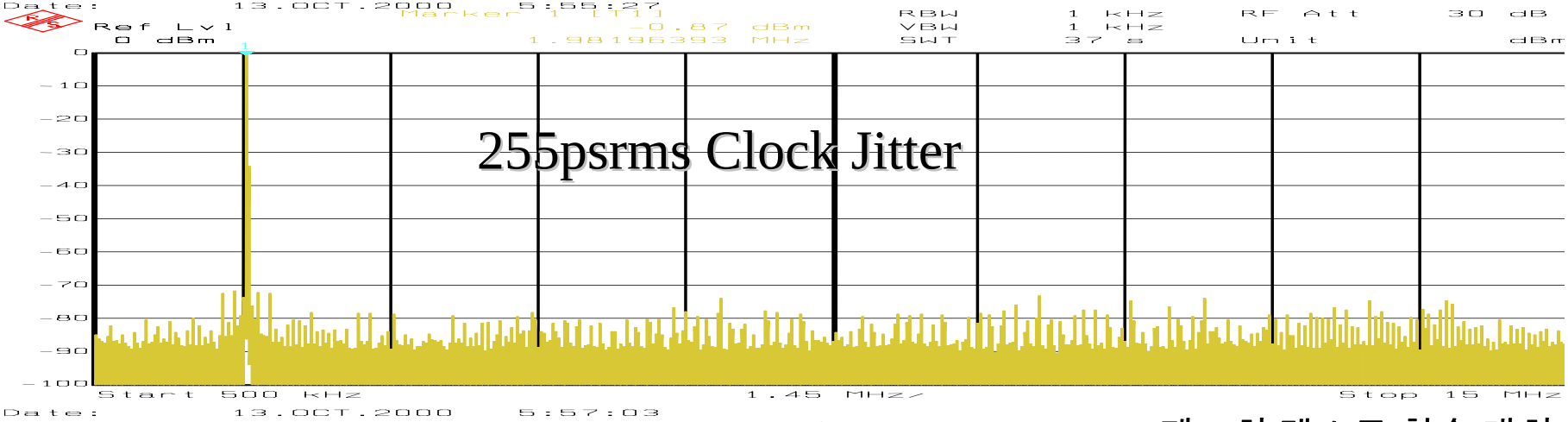
Fi 10Mhz , Clock Jitter 255psrms
Power Spectrum of 14 bit ADC



Fi 2Mhz , Clock Jitter 20psrms & 255psrms for 14 bit ADC

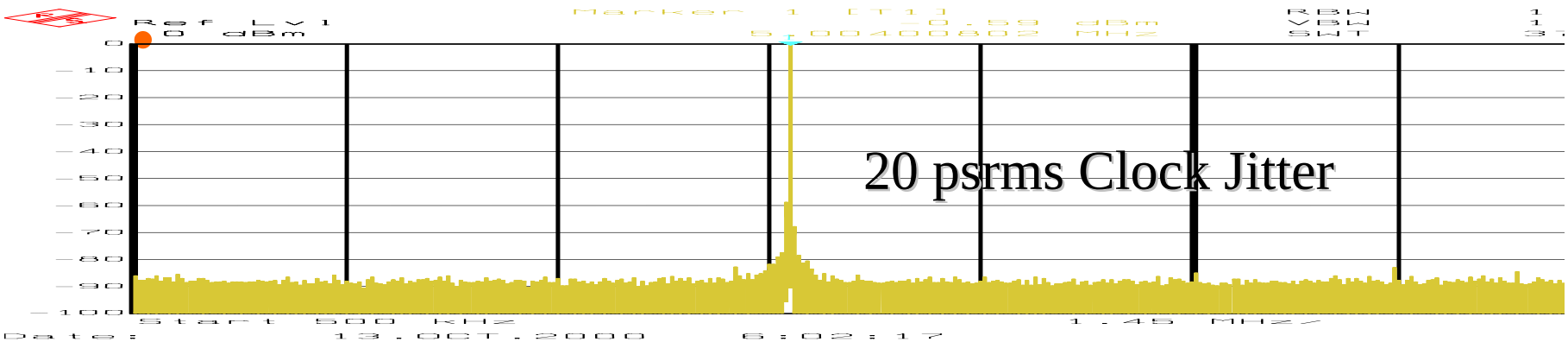


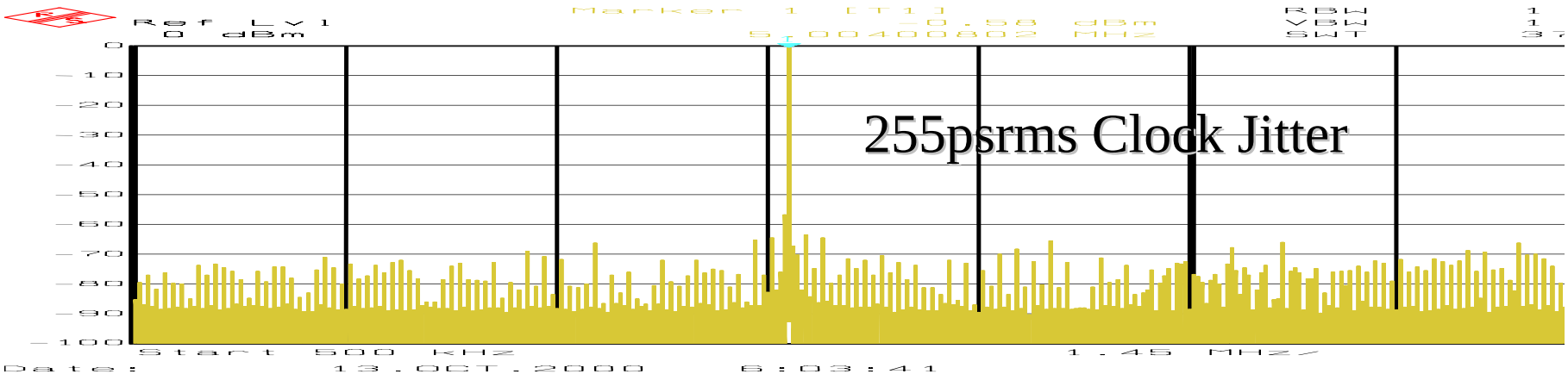
20 psrms Clock Jitter



255psrms Clock Jitter

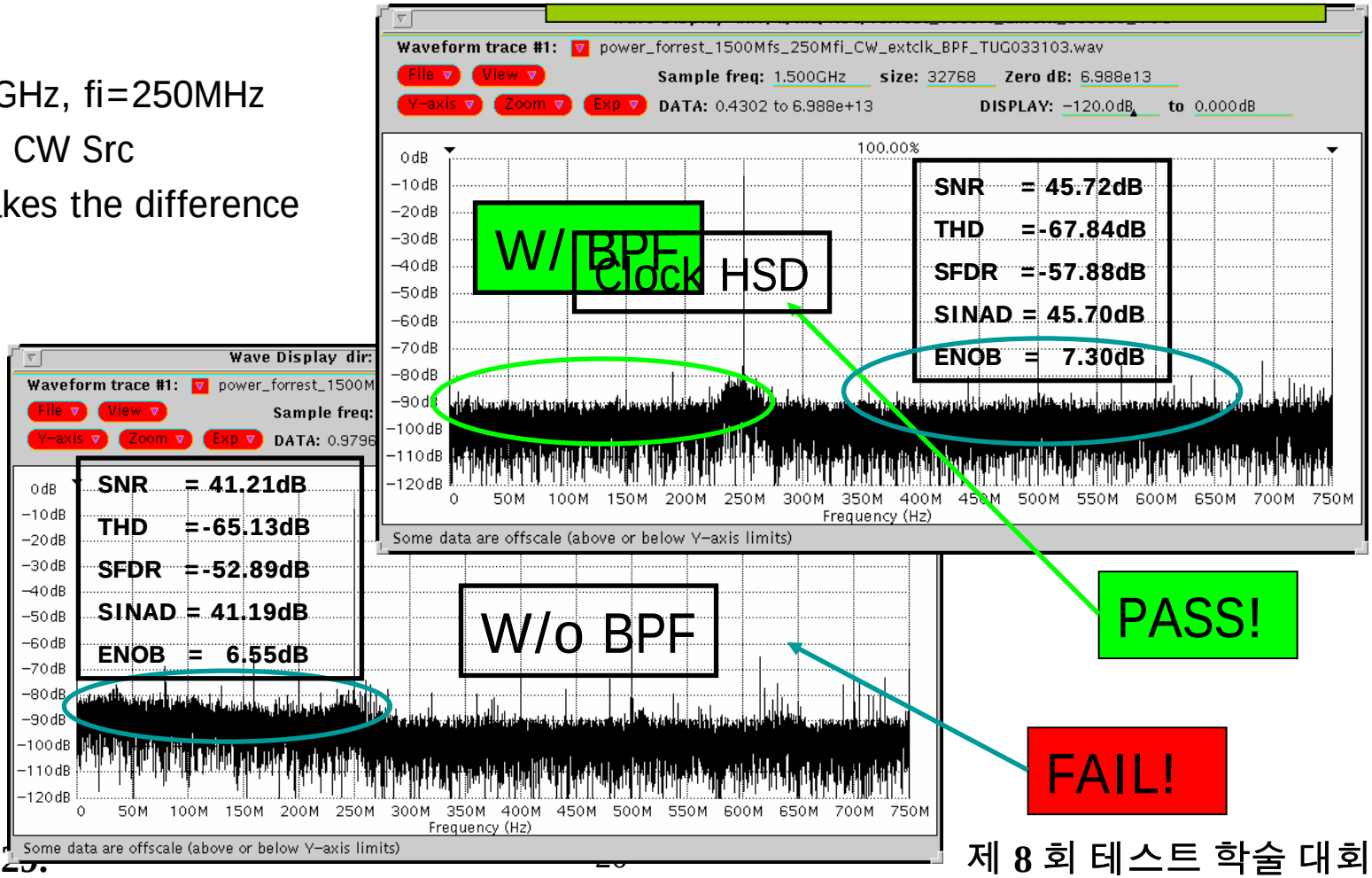
Fi=5Mhz , Clock Jitter 20psrms & 255psrms for 14 bit ADC





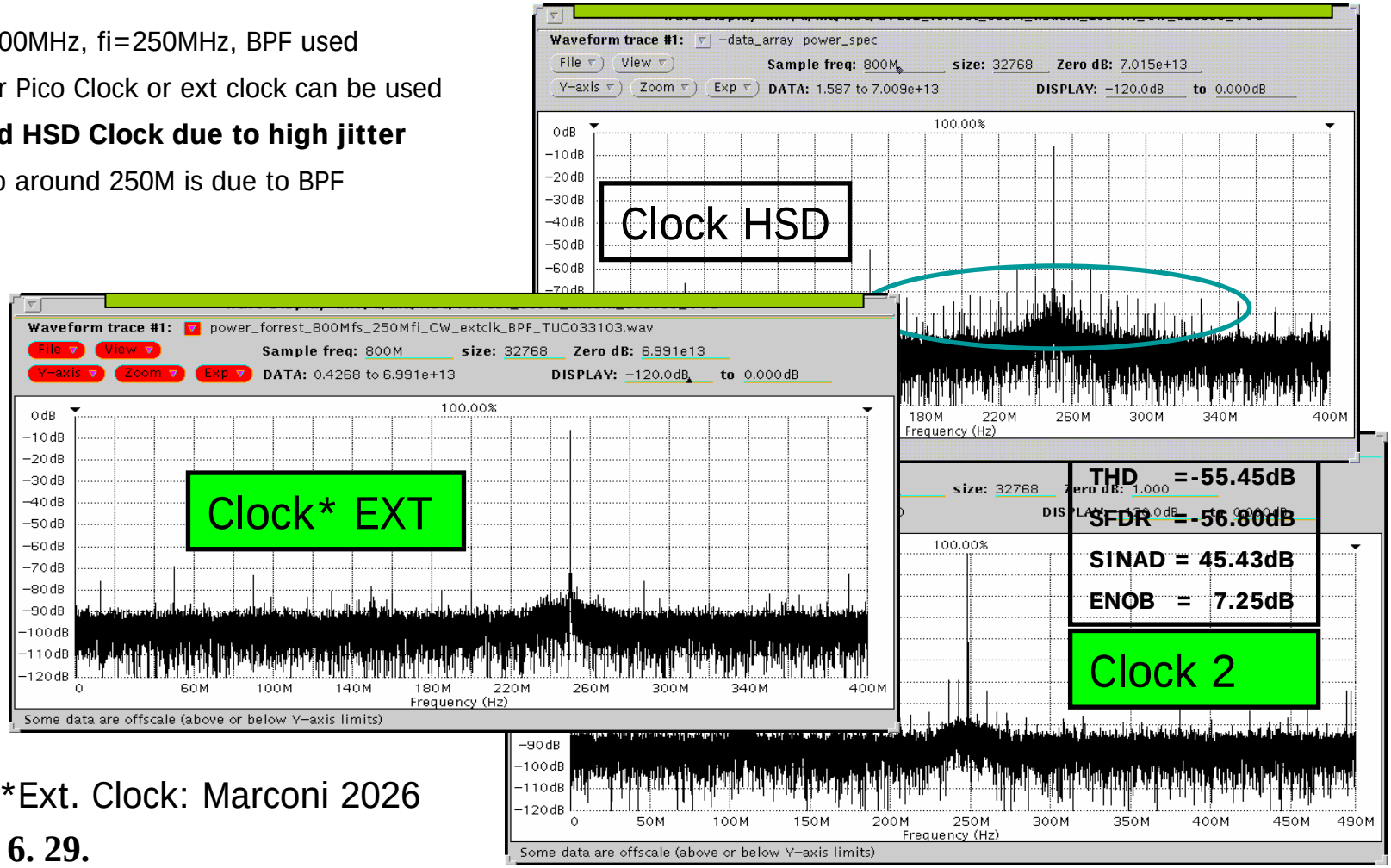
Signal Filtering Effect by BPF

- Fs=1.5GHz, fi=250MHz
- Ext Clk, CW Src
- BPF makes the difference



Fi = 250Mhz, Fs=800Mhz : Clock Jitter Performance Test

- Fs=800MHz, fi=250MHz, BPF used
- Either Pico Clock or ext clock can be used
- **Avoid HSD Clock due to high jitter**
- Bump around 250M is due to BPF

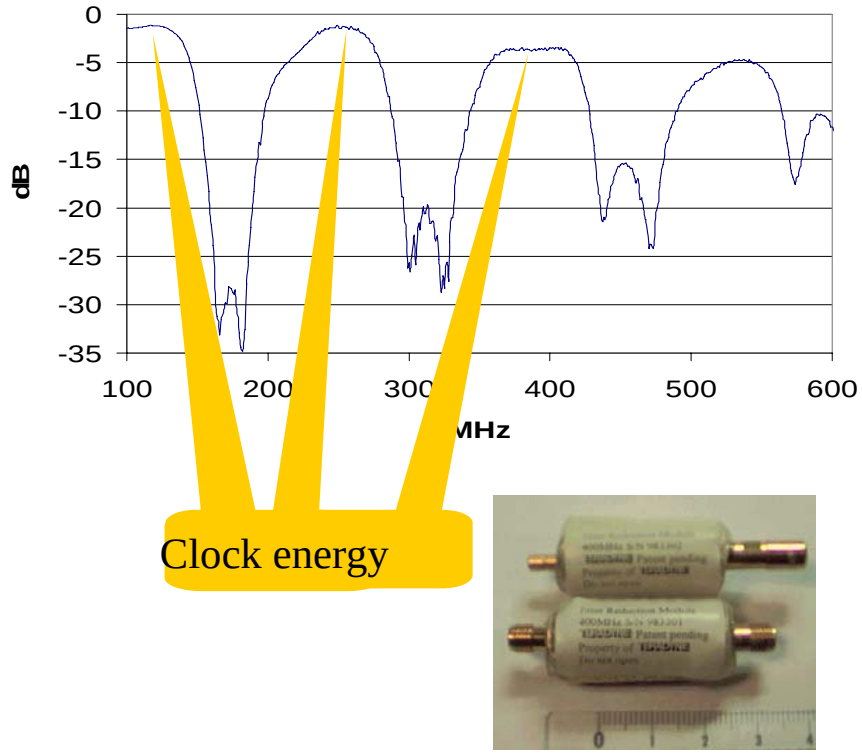


*Ext. Clock: Marconi 2026

2007. 6. 29.

Reduce Jitter Effect

- Pick a Low Jitter Clock Source (Pico-Clk, HP8644B)
- Use the Instrument in “Low Jitter Condition”- DIB Design
- Use Narrow BPF if Device Accept Sinewave as Clock
- Use Jitter Reduction Module



Q&A?